Amendments to the Drawings:

Add new drawing Fig. 6. The applicant has included new figure 6 having the identification "new sheet" located in the top margin.

Attachment: New Sheet 1 page(s)

REMARKS/ARGUMENTS

1. A new figure, Fig. 6, showing the implementation of the claimed invention is submitted as an informal drawing for consideration. The basis of Fig. 6 can be found in paragraph [0021] of the detailed specification, specially "Since the leakage current problems are more sensitive around the drain, **the leakage currents can be reduced by overlapping a edge of the gate 50 with the lightly doped drain adjacent to the drain, and preventing the edge of the gate 50 from overlapping with either of the junction between the drain and the lightly doped drain or the drain. In addition, whether it is necessary to overlap the other edge of the gate 50 with the lightly doped drain adjacent to the source and keep it away from the junction between the lightly doped drain and the source or not can be an optional design choice** according to the device characteristic demands of the transistor." No new matter is introduced. At this time, the specification has not been amended to include the references to the new figure.

2. Claims 1-2, 4, 5, and 7-15 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,558,993 to Ohtani et al.

Response:

Claims 1-8 are cancelled, and are no longer in need of consideration.

Regarding claim 9, claim 9 recites a thin-film transistor comprising a substrate, a semiconductor layer positioned on the substrate, the semiconductor layer comprising a channel region, two lightly doped drains, a source and a drain. The thin-film further comprises an insulating layer

positioned on the semiconductor layer and a gate positioned on the insulating layer, the gate comprising *a gate edge overlapped with the lightly doped drain adjacent to the drain, the gate being not overlapped with the junction between the lightly doped drain, and the gate being not overlapped with the drain.*

In general, the leakage currents are generated because a voltage remains between the drain and the substrate when the transistor is off, and the leakage current problems are more sensitive around the drain. **Therefore, the leakage currents can be effectively reduced by only overlapping an edge of the gate with the lightly doped drain adjacent to the drain, and preventing the edge of the gate from overlapping with either of the junction between the drain and the lightly doped drain or drain.** In addition, whether the gate overlaps with the lightly doped drain adjacent to the source and keeps away from the junction between the lightly doped drain and the source or not can be an optional design choice.

Contrary to the present application, Ohtani's LDD regions 108 are all overlapped by the gate electrode 105 according to Figs 1-4. It is obvious that Ohtani did not consider that the leakage currents are more sensitive around the drain thus it can be effectively reduced by only overlapping the gate electrode with the LDD region adjacent to the drain. **Both edges of the gate electrode 105 disclosed by Ohtani are made overlapping with the lightly doped drains adjacent to the drain/source while the gate provided by the present application has its only one edge overlapped with the lightly doped drain adjacent to the drain.** The applicant asserts that claim 9 is patentably distinct from Ohtani, therefore reconsideration of

claim 9 is politely requested.

Claims 10-15 are dependent on claim 9 and should be allowed if claim 9 is allowed.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,558,993 to Ohtani et al., in view of Yeh et al.

Response:

Claim 3 is cancelled, and is no longer in need of consideration.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 03/23/2006

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)